UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,030	03/19/2001	Rong Lin	87687.042301/R-1265-125	9309

34799 7590 06/16/2005

THOMAS R. FITZGERALD, ESQ.
16 E. MAIN STREET, SUTIE 210
ROCHESTER, NY 14614-1803

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/812,030	LIN, RONG	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-26 and 28-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-26,28-45 and 58-60* is/are allowed.

6)☒ Claim(s) *46-48, 50-52, 54-56* is/are rejected.

7)☒ Claim(s) *49,53 and 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 04/19/2005.

2. Claims 4-26 and 28-60 are pending in this application. Claims 4, 6, 12-14, 28, 32, 39, 43, 46, and 58 are independent claims. This Office Action is made final.

Claim Objections

3. Claim 53 is objected to because of the following informalities:

This claim is in dependent form of itself. For examination purposes, the examiner considers claims 53 and 57 depending on claim 49. The applicant is required to correct this issue in the next Office action.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 46-48, 50-52, and 54-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Hung et al. (U.S. 6,530,010).

Re claim 46, Hung et al. disclose a reconfigurable matrix multiplier circuit for multiplying two mathematical matrices (abstract lines 1-7 and col. 9 lines 17-20) comprising: an input network of multipliers (Figures 25-26) connected to input bit signal lines (e.g. inputs into 4x4 matrix) for generating partial product output signals representative of the partial products of two multiplied mathematical matrices: a first output network of adders (col. 16 lines 22-25; col. 12 lines 19-24; and col. 8 lines 29-30) and a second output network of accumulators (col. 16 lines 1-7 and col. 2 lines 12-18) and a plurality of configuration control switches (col. 9 lines 57-62) coupled to the multipliers and to output networks and selectively operable between first and second state to connect the partial product output signals of the multipliers to the output network of adders when the control switches are in their first state (col. 16 lines 22-25) and for connecting the partial product output signals of the multipliers to the output network of accumulators when the control switches are in their second state (col. 16 lines 1-7).

Re claim 47, Hung et al. further disclose the control switches in their first state couple the outputs of the multipliers to the output adder network for generating multiple mathematical matrix partial products (e.g. col. 12 line 22 and col. 16 lines 20-25) and the control switches in their second state couple the outputs of the multipliers to the output accumulator network to generate a signal mathematical matrix partial product (col. 20 lines 11-15).

Re claim 48, Hung et al. further disclose a plurality of the composite reconfigurable matrix multiplier circuits (e.g. Figure 25).

Re claims 50-52, Hung et al. further disclose a set of four smaller identical reconfigurable matrix multiplier circuits each multiplying two 32/16/8-bit numbers or two 8x8/4x4/2x2 matrices respectively (Figures 25-26 and col. 9 lines 38-52 and col. 15 lines 4-10).

Re claims 54-56, Hung et al. further disclose a pair of one-bit controlled 64-bit switches enabling the matrix multiplier circuit to multiply either two 64/32/16-bit numbers or two 16x16/8x8/4x4 matrices respectively (Figures 25-26 and col. 9 lines 38-52 and col. 15 lines 4-10).

Allowable Subject Matter

6. Claims 4-26, 28-45, and 58-60 are allowed.

7. Claims 49, 53, and 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 04/19/2005 have been fully considered but they are not persuasive.

a. The applicant argues in page 15 second paragraph for claim 46 that the cited reference does not have the claimed arrays and switches. In addition, the cited reference does not express or teach the used of the same multiplier array to perform both conventional and matrix multiplication.

The examiner respectfully submits that Figures 13a-13b show the switches as multiplexers (e.g. 359, 369...in Figure 13b) and the process data is in array format as seen in Figure 18. The claim language of claim 46 does not clearly require or define the same multiplier array to perform both conventional and matrix multiplication.

b. The applicant argues in page 15 third paragraph for claim 46 that the cited reference does not disclose control switches connected between multipliers and arrays of adders or accumulators.

The examiner respectfully submits that Figures 13a-13b show the control switches as multiplexers (e.g. 369 in Figure 13b) for connecting the output of multipliers (e.g. output of 374 in Figure 13b) to the accumulator or adder (e.g. 368 in Figure 13b).

c. The applicant argues in page 15 fourth paragraph for claim 46 that the cited reference does not disclose an instance of where the output of the multiplier goes to an accumulator before going to an adder.

The examiner respectfully submits that the claim language of claim 46 does not clearly require or define the output of the multiplier goes to an accumulator before going to an adder as argued.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the same multiplier array to perform both conventional and matrix multiplication" in the second paragraph page 15 and "the output of the multiplier goes to an accumulator before going to an adder" as cited in the fourth paragraph page 15) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

June 4, 2005

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 210